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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,466	KASUGA ET AL.	
	Examiner	Art Unit	
	Nelson D. Hernández Hernández	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,13-19 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-19,22 and 23* is/are allowed.

6)☒ Claim(s) *1-8,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on November 13, 2008 has been entered.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Response to Amendment

3. The Examiner acknowledges the amended claims filed on November 13, 2008. **Claim 1** has been amended. **Claims 9-12, 20 and 21** have been cancelled.

Response to Arguments

4. Applicant's arguments with respect to **claim 1** have been considered but are moot in view of the new grounds of rejection based on additional teaching of previously presented prior art on record.

5. Applicant's arguments filed November 13, 2008 have been fully considered but they are not persuasive. The Applicant further argues the following:

a. Based on the foregoing description, Applicants note that while Koizumi discloses the ability to input a high level pulse RST to the reset switch Q2 and a high level pulse to the gate transfer switch Q 1, that Koizumi does not teach, suggest or otherwise render obvious the features of an electric charge simultaneous removal unit that includes timing generation circuits each having: a first switch transistor that serves as a switch; a capacitor disposed between a gate and a drain of the first switch transistor; and a second switch transistor connected to the gate of the first switch transistor, wherein charging the capacitor prevents a voltage drop in the reset signal applied from a source of the first switch transistor of one of the timing generation circuits and in the readout signal applied from a source of the first switch transistor of another one of the timing generation circuits, and wherein the reset signal is applied to a gate of the reset transistor, and the readout signal is applied to a gate of the readout transistor, each of the reset signal and the readout signal reaching a high level and maintaining the high level for the same period of time, and the reset transistor

and the readout transistor being included in each of the photoelectric conversion circuits disposed in the region to be read out, as recited in amended claim 1.

- The Examiner noted that Koizumi does not teach the features of an electric charge simultaneous removal unit that includes timing generation circuits each having: a first switch transistor that serves as a switch; a capacitor disposed between a gate and a drain of the first switch transistor; and a second switch transistor connected to the gate of the first switch transistor, wherein charging the capacitor prevents a voltage drop in the reset signal applied from a source of the first switch transistor of one of the timing generation circuits and in the readout signal applied from a source of the first switch transistor of another one of the timing generation circuits. However, the above mentioned limitations are taught by the Applicants Admitted Prior Art as will be discussed with regards to claim 1 in this Office Action.

- Also as will be discussed in the rejections made to claim 1 in this Office Action, Koizumi discloses the reset signal is applied to a gate of the reset transistor, and the readout signal is applied to a gate of the readout transistor, each of the reset signal and the readout signal reaching a high level and maintaining the high level for the same period of time, and the reset transistor and the readout transistor being included in each of the photoelectric conversion circuits disposed in the region to be read out, as recited in amended claim 1. The Examiner noted that the limitations “each of the reset signal and the readout signal reaching a high level and maintaining the high level for the same period of

time" do not require that both the reset signal and the readout signal occur simultaneously. The Examiner understands that the limitations as written can be interpreted as having each of the reset signal and the readout signal reaching a high level and maintaining the high level for the same durations of time, thus that both, the reset signal and the readout signal even when occurring at different cycles, both have the same period (duration) of time. Therefore, as shown in figs. 2 and 4, Koizumi et al. further discloses that each of the reset signal and the readout signal reaching a high level and maintaining the high level for the same period of time (Note that the reset signal and the readout signal both reach a high level and maintain said high level for the same period (duration or amount) of time as shown in figs. 2 and 4), and the reset transistor and the readout transistor being included in each of the photoelectric conversion circuits disposed in the region to be readout (Note that every photoelectric conversion circuit includes a reset transistor and a readout transistor as shown in fig. 9. This teaches that the reset transistor and the readout transistor are included in each of the photoelectric conversion circuits disposed in the region to be readout as claimed).

b. "For example, regarding Satoshi, Applicants note that this reference discloses the use of a solid state imaging device 3 having a mechanical shutter 2 arranged thereon (see Fig. 3 and Abstract). As explained in Satoshi, exposure of the imaging device is started by simultaneously resetting all of the pixels of the

imaging device 3 in the state of opening the mechanical shutter 2 (see Abstract and paragraph [0011]). Regarding the AAPA, as shown in Fig. 3, a timing generation circuit includes a bootstrap circuit 146 that functions as a capacitor, and a transistor 148. As explained on page 3 of the specification, when electric charge is accumulated in the bootstrap circuit 146, a reset signal RSCELL is output to a reset transistor of each pixel.

Based on the foregoing, Applicants note that while (1) Satoshi discloses starting exposure by simultaneously resetting all of the pixels of the imaging device 3 in the state of opening the mechanical shutter 2, and (2) the AAPA discloses the use of a capacitor and switch transistor 148 that enables a reset signal to be output to each pixel, that Satoshi and the AAPA do not teach, suggest or otherwise render obvious the features of an electric charge simultaneous removal unit that includes timing generation circuits each having: a first switch transistor that serves as a switch; a capacitor disposed between a gate and a drain of the first switch transistor; and a second switch transistor connected to the gate of the first switch transistor, wherein charging the capacitor prevents a voltage drop in the reset signal applied from a source of the first switch transistor of one of the timing generation circuits and in the readout signal applied from a source of the first switch transistor of another one of the timing generation circuits, and wherein the reset signal is applied to a gate of the reset transistor, and the readout signal is applied to a gate of the readout transistor, each of the reset signal and the readout signal reaching a high level and

maintaining the high level for the same period of time, and the reset transistor and the readout transistor being included in each of the photoelectric conversion circuits disposed in the region to be read out, as recited in amended claim 1."

- The Examiner disagrees. As will be explained in this Office Action in regards to claim 1, the AAPA teaches the features of an electric charge simultaneous removal unit (timing generation unit as shown in AAPA, fig. 3) that includes timing generation circuits each having: a first switch transistor (AAPA; fig. 3: 148) that serves as a switch; a capacitor (AAPA, fig. 3: 146) disposed between a gate and a drain of the first switch transistor; and a second switch transistor (AAPA; fig. 3, transistors 142 and 144) connected to the gate of the first switch transistor (See AAPA, fig. 3), wherein charging the capacitor prevents a voltage drop in the reset signal applied from a source of the first switch transistor of one of the timing generation circuits (See AAPA, page 3, line 13 – page 4, line 15) and in the readout signal applied from a source of the first switch transistor of another one of the timing generation circuits (Col. 4, line 47 – col. 5, line 2) wherein the reset signal is applied to a gate of the reset transistor (See AAPA, fig. 1), and the readout signal is applied to a gate of the readout transistor (See AAPA, fig. 1).

- The Examiner understands that AAPA fails to teach that each of the reset signal and the readout signal reaching a high level and maintaining the high level for the same period of time, and the reset transistor and the readout transistor being included in each of the photoelectric conversion circuits disposed in the

region to be read out, as recited in amended claim 1. However, as explained above, those features are discloses in the Koizumi et al. reference.

6. Therefore, the Examiner understands that all the limitations of claim 1 as now amended are taught by the combined teaching of Koizumi et al. in view of AAPA as will be discussed below.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-3, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al., US Patent 7,015,964 B1 in view of Applicant Admitted Prior Art (AAPA).

Regarding claim 1, Koizumi et al. discloses a solid-state image sensing apparatus (See fig. 1, 9 and 10) for performing photoelectric conversion of incident light, the solid-state image sensing apparatus comprising:

a photosensitive unit (See fig. 10) in which a plurality of photoelectric conversion circuits (Figs. 1, 9: PX and 10: PX1, PX2, PX3, PX4) are arranged one-dimensionally or two-dimensionally (See fig. 10), each of the photoelectric conversion circuits corresponding to one of a plurality of pixels, and each of the photoelectric conversion circuits including a photodiode (Figs. 1: PD, 9: PD) for accumulating electric charge by

performing the photoelectric conversion of incident light and an output circuit for outputting the accumulated electric charge as an electric signal (Col. 4, line 47 – col. 5, line 2);

an electric charge simultaneous removal unit (Fig. 1: SCC) operable to simultaneously remove the accumulated electric charge in each of the photodiodes disposed in a predetermined region to be read out in the photosensitive unit (Col. 7, lines 3-47); and

an electric charge accumulation unit (charge is accumulated in photodiode PD by operation of the SCC) operable to accumulate electric charge in each of the photodiodes disposed in the region to be read out during a predetermined time after the accumulated electric charge in each of the photodiodes disposed in the region to be read out is removed (Col. 5, lines 25-43; col. 7, lines 3-64),

wherein the output circuit in each of the photoelectric conversion circuits includes:

a readout transistor (Fig. 1: Q1) for receiving a readout signal from the electric charge simultaneous removal unit (Fig. 1: SCC) and which allows the electric charge accumulated in the photodiode to pass therethrough in response to activation of the readout signal (Col. 4, lines 47-61; col. 5, line 25 – col. 6, line 11);

an electric charge retention unit (Fig. 1: FD) operable to receive the electric charge that passes through the readout transistor and to retain the electric charge (col. 5, line 25 – col. 6, line 11; col. 7, lines 3-67);

an amplifier transistor (Fig. 1: Q3) which allows the electric signal to pass therethrough, the electric signal being based on a value of voltage determined by the electric charge retained by the electric charge retention unit (Col. 4, lines 47-61; col. 5, line 21 – col. 6, line 11; col. 7, lines 3-67); and

a reset transistor (Fig. 1: Q2) for receiving a reset signal from the electric charge simultaneous removal unit (Fig. 1: SCC) and for resetting an amount of electric charge accumulated in the electric charge retention unit in response to activation of the reset signal (Col. 4, lines 47-61; col. 5, line 21 – col. 6, line 11; col. 7, lines 3-67), and

wherein the reset signal is applied to a gate of the reset transistor (Note that the reset signal øRST is applied to the gate of the reset transistor Q2 as shown in fig. 1), and the readout signal is applied to a gate of the readout transistor (Note that the readout signal øTX is applied to the gate of the readout transistor Q1 as shown in fig. 1), each of the reset signal and the readout signal reaching a high level and maintaining the high level for the same period of time (The Examiner noted that the limitations “each of the reset signal and the readout signal reaching a high level and maintaining the high level for the same period of time” do not require that both the reset signal and the readout signal occur simultaneously. The Examiner understands that the limitations as written can be interpreted as having each of the reset signal and the readout signal reaching a high level and maintaining the high level for the same durations of time, thus that both, the reset signal and the readout signal even when occurring at different

cycles, both have the same period (duration) of time. Therefore, as shown in figs. 2 and 4, Koizumi et al. further discloses that each of the reset signal and the readout signal reaching a high level and maintaining the high level for the same period of time (Note that the reset signal and the readout signal both reach a high level and maintain said high level for the same period (duration or amount) of time as shown in figs. 2 and 4)), and the reset transistor and the readout transistor being included in each of the photoelectric conversion circuits disposed in the region to be readout (Note that every photoelectric conversion circuit includes a reset transistor and a readout transistor as shown in fig. 9. This teaches that the reset transistor and the readout transistor are included in each of the photoelectric conversion circuits disposed in the region to be readout as claimed).

Although Koizumi et al. teaches the use of an electric charge simultaneous removal unit (Fig. 1: SCC) having at least a timing generation circuit (this is inherently taught in Koizumi et al., since the use of at least a timing generation circuit is needed for proper operation of the control circuit SCC), Koizumi et al. does not goes into details of the structure of said electric charge simultaneous removal unit. Koizumi et al. does not explicitly disclose that said electric charge simultaneous removal unit includes a plurality of timing generation circuits each having: a first switch transistor that serves as a switch; a capacitor disposed between a gate and a drain of the first switch transistor; and a second switch transistor connected to the gate of the first switch transistor, wherein charging the capacitor prevents a voltage drop in the reset signal applied from a source

of the first switch transistor of one of the timing generation circuits and in the readout signal applied from a source of the first switch transistor of another one of the timing generation circuits.

However, AAPA discloses a solid-state image sensing apparatus (Fig. 1) that performs photoelectric conversion of incident light, comprising:

a photosensitive unit (See fig. 1) in which a plurality of photoelectric conversion circuits (Fig. 1: 112) is laid out one-dimensionally or two-dimensionally, each of said photoelectric conversion circuits corresponding to a pixel and including a photodiode that accumulates electric charge by performing the photoelectric conversion of incident light and an output circuit that outputs the accumulated electric charge as an electric signal;

an electric charge removal unit (timing generation unit) operable to remove the accumulated electric charge in the photodiodes laid out in a predetermined region to be read out in the photosensitive unit; and

an electric charge accumulation unit (Fig. 2: 128) operable to accumulate electric charge in the photodiode laid out in the region to be read out during a predetermined time after the accumulated electric charge in the photodiode that is laid out in the region is removed. AAPA also discloses that the electric charge simultaneous removal unit includes:

a first switch transistor (AAPA; fig. 3: 148) that serves as a switch;

a capacitor (AAPA, fig. 3: 146) that is set up between a gate and a drain of the switch transistor, and

a second switch transistor (AAPA; fig. 3, transistors 142 and 144) connected to the gate of the first switch transistor (See AAPA, fig. 3), wherein charging the capacitor prevents a voltage drop in the reset signal applied from a source of the first switch transistor of one of the timing generation circuits (See AAPA, page 3, line 13 – page 4, line 15) and in the readout signal applied from a source of the first switch transistor of another one of the timing generation circuits (See AAPA, page 3, line 13 – page 4, line 15) (See also, page 1, lines 11-32; page 2, line 1 – page 6, line 1).

The configuration of the electric charge simultaneous removal unit as taught in AAPA is advantageous because it would allow resetting all the pixels simultaneously thus avoiding uneven collection of image signal that would result in unwanted noise.

Therefore, taking the combined teaching of Koizumi et al. in view of AAPA as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to apply the configuration shown for the electric charge simultaneous removal unit as taught in AAPA on the electric charge simultaneous removal unit of Koizumi et al. by having a switch transistor that serves as a switch; and a capacitor that disposed between a gate and a source or a drain of the switch transistor, and wherein, when the capacitor is charged, the reset signal is inputted from the drain of the switch transistor and is outputted simultaneously to all of the photoelectric conversion circuits from the source. The motivation to do so would have been to improve the operation of the solid state imaging device by allowing to reset all the pixels simultaneously thus avoiding uneven collection of image signal that would result in unwanted noise.

Regarding claim 2, Koizumi et al. discloses that the electric charge accumulation unit (SCC) generates an electric accumulation start signal to start electric charge accumulation to for each of the photodiodes disposed in the region to be read out (Col. 4, lines 47-61; col. 5, line 21 – col. 6, line 11; col. 7, lines 3-67).

Regarding claim 3, Koizumi et al. discloses that the electric charge accumulation unit generates an electric accumulation end signal and ends electric charge accumulation for each of the photodiodes disposed in the region to be read out in response to activation of the electric charge accumulation end signal (col. 5, line 21 – col. 6, line 11).

Regarding claim 24, Koizumi et al. discloses that the electric charge simultaneous removal unit aligns a pulse of the reset signal and a pulse of the readout signal (Col. 3, lines 1-20; col. 4, lines 47-61; col. 5, line 21 – col. 6, line 11; col. 7, lines 3-67).

Regarding claim 25, Koizumi et al. discloses that the reset signal having a width of a pulse that is wider than a width of a pulse of the readout signal (Col. 3, lines 1-20; col. 4, lines 47-61; col. 5, line 21 – col. 6, line 11; col. 7, lines 3-67; See also figs. 2 and 8).

9. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi et al., US Patent 7,015,964 B1 in view of Applicants Admitted Prior Art (AAPA) and further in view of Satoshi et al., JP 2000-078484 A.

Regarding claim 4, the combined teaching of Koizumi et al. in view of AAPA fails to teach an incident light control unit operable to control incidence of light into the photosensitive unit, wherein the electric charge accumulation unit ends electric charge accumulation to each of the photodiode laid out photodiodes disposed in the region to be read out using the incident light control unit by blocking out incidence of light into the photosensitive unit.

However, Satoshi et al. discloses a solid-state image sensing apparatus (Fig. 1) that performs photoelectric conversion of incident light, comprising: a photosensitive unit (Fig. 1: 3) in which a plurality of photoelectric conversion circuits is laid out one-dimensionally or two-dimensionally (English Translation, Page 3, ¶ 0008), each of said photoelectric conversion circuits corresponding to a pixel and including a photodiode that accumulates electric charge by performing the photoelectric conversion of incident light and an output circuit that outputs the accumulated electric charge as an electric signal (See fig. 2; English Translation, page 3, ¶ 0009); an electric charge simultaneous removal unit (Fig. 1: 8) operable to simultaneously remove the accumulated electric charge in the photodiodes laid out in a predetermined region to be read out in the photosensitive unit. Satoshi et al. also teaches an incident light control unit (Satoshi et al., CPU 8 controls the mechanical shutter 2; see fig. 1) positioned between the photosensitive unit and the object to be photographed and is operable to control

incidence of light into the photosensitive unit, wherein the electric charge accumulation unit ends electric charge accumulation to the photodiode laid out in the region to be read out using the incident light control unit by blocking out incidence of light into the photosensitive unit (Satoshi et al., English Translation, page 3, ¶ 0008-0009; page 4, ¶ 0011 – page 5, ¶ 0016).

Therefore, taking the combined teaching of Koizumi et al. in view of AAPA and further in view of Satoshi et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching of Koizumi et al. and AAPA by having an incident light control unit operable to control incidence of light into the photosensitive unit, wherein the electric charge accumulation unit ends electric charge accumulation to each of the photodiode laid out photodiodes disposed in the region to be read out using the incident light control unit by blocking out incidence of light into the photosensitive unit. The motivation to do so would have been to allow the solid state image sensing device to expose all the photodiodes to start colleting image signal and to terminate exposure to all photodiodes globally thus better performing exposure control at a high speed on real time.

Regarding claim 5, the combined teaching of Koizumi et al. in view of AAPA and further in view of Satoshi et al. as discussed and analyzed in claim 4 teaches an incident light control unit (Satoshi et al., CPU 8 controls the mechanical shutter 2; see fig. 1) operable to control incidence of light into the photosensitive unit, wherein the electric charge accumulation unit starts incidence of light to the photosensitive unit

using the incident light control unit after the electric charge simultaneous removal unit simultaneously removes the accumulated electric charge for each the photodiodes disposed in the region to be read out (After the reset signal is made, the exposure starts by opening a shutter (Satoshi et al., fig. 1: 2) to have the pixels accumulate charge signal and after the exposure signal is made, a signal to close a mechanical shutter (Satoshi et al., fig. 1: 2) to stop accumulating image signal and the accumulated signal is read; Satoshi et al., English Translation, page 4, ¶ 0011 – page 5, ¶ 0016).

Regarding claim 6, limitations can be found in claim 4.

Regarding claim 7, limitations can be found in claim 4.

Regarding claim 8, the combined teaching of Koizumi et al. in view of AAPA and further in view of Satoshi et al. fails to teach that the incident light control unit includes: a liquid crystal shutter disposed between the photosensitive unit and an object to be photographed; and a liquid crystal shutter control unit operable to apply a predetermined voltage to the liquid crystal shutter to control a penetration of light.

However, Official Notice is taken that the use of liquid crystal shutter set up between the photosensitive unit and an object to be photographed controlled by applying a predetermined voltage to the liquid crystal shutter to control a penetration of light is well known in the art and one of an ordinary skill in the art would be motivated to change the mechanical shutter in Satoshi et al. with a liquid crystal shutter with the

motivation of reducing the power drain of the mechanical shutter and also to reduce the complexity and size of the imaging device.

Allowable Subject Matter

10. **Claims 13-19, 22 and 23** are allowed.

11. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 13, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest, including all the elements of the present claim, an electric signal readout unit operable to read out the electric signals outputted from the photoelectric conversion circuits disposed in the region to be read out, wherein the electric signal readout unit includes: a first unit operable to output the activated reset signal to the each of the reset circuits in the photoelectric conversion circuits disposed in the region to be read out; and a second unit operable to output the activated readout signal to each of the reset circuits disposed in the region to be read out after outputting the reset signal, and wherein the first unit outputs the activated reset signal after the predetermined time in the electric charge accumulation unit has passed.

Regarding claim 17, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest, including all the elements of the present claim, an electric signal readout unit operable to read out the electric signals outputted from the photoelectric conversion circuits disposed in the region to be read

out, wherein the electric signal readout unit includes: a first unit operable to output the activated reset signal to each of the reset circuits in the photoelectric conversion circuits disposed in the region to be read out; and a second unit operable to output the activated readout signal to each of the reset circuits disposed in the region to be read out after outputting the reset signal, and wherein the first unit outputs the activated reset signal before the predetermined time in the electric charge accumulation unit has passed.

Regarding claim 19, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest, including all the elements of the present claim, an electric signal readout unit operable to read out the electric signals outputted from the photoelectric conversion circuits disposed in the region to be read out, wherein the electric signal readout unit includes: a first unit operable to output the activated reset signal to each of the reset circuits in the photoelectric conversion circuits disposed in the region to be read out; and a second unit operable to output the activated readout signal to each of the reset circuits after outputting the reset signal, and wherein the first unit outputs the activated reset signal for a period starting from a mid point of the predetermined time until an end of the predetermined time in the electric charge accumulation unit.

Regarding claim 22, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest, including all the elements of the present claim, that the electric charge simultaneous removal unit includes: a first

switch transistor that serves as a switch; a capacitor disposed between a gate and a source or a drain of the first switch transistor; and a second switch transistor that serves as a switch, wherein the second switch transistor receives an all pixel reset switch signal and an all pixel reset signal, wherein the capacitor is charged during a time period in which the all pixel reset switch signal and the all pixel reset signal are input to a gate and a drain, respectively, of the second switch transistor, and wherein, when the capacitor is charged, the reset signal is input to the drain of the first switch transistor and is output simultaneously to all of the photoelectric conversion circuits from the source of the first switch transistor.

Regarding claim 23, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest, including all the elements of the present claim, that wherein the electric charge simultaneous removal unit includes: a first switch transistor that serves as a switch; a capacitor disposed between a gate and a source or a drain of the first switch transistor; and a second switch transistor that serves as a switch, wherein the second switch transistor receives an all pixel reset switch signal and an all pixel reset signal, wherein the capacitor is charged during a time period in which the all pixel reset switch signal and the all pixel reset signal are input to a gate and a drain, respectively, of the second switch transistor, and wherein, when the capacitor is charged, the reset signal is input to the drain of the first switch transistor and is output simultaneously to all of the photoelectric conversion circuits from the source of the first switch transistor.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson D. Hernández Hernández whose telephone number is (571)272-7311. The examiner can normally be reached on 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nelson D. Hernández Hernández
Examiner
Art Unit 2622

NDHH
December 9, 2008

/Lin Ye/
Supervisory Patent Examiner, Art Unit 2622